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Simulation & Analysis of 10-Stage Delay Line using CNT Transistor at 32nm

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Abstract:- In this article the equivalent study of discrete parameters of delay line by using CMOS and CNT techniquesare done. After the comparative study the results exhibited that the CNT displayed better results as compared to the CMOS 10 stages delay line at 32nm technology design. Two parameters propagation delay and average power consumption are also calculated andcompared. After the comparison of parameters it is found that CNT delay line has better results as compared to CMOS delay line. The power consumption is also decreased in the Delay line by using CNT as compared to CMOS delay line. During simulation it is found that the propagation delay of CNT delay line reduced by 4.06% then CMOS delay line. Similarly it is also measured during simulation that avg. power consumption of CNT delay line reduced by 20.99% as compared to CMOS delay line. However Voltage using during both type of material is similar and fixed at 0.9v.

Keyword:- *Carbon nanotube, CMOS, Delay line, Power consumption, Propagation delay etc.*

I. INTRODUCTION

In this article, it describes a delay line circuit which can be used for different types of applications. Specifically, we have built closed loop when is able to create various clock phases and delays with low jitter, short locking time, and wide lock range. To achieve this design goal, several techniques and algorithms are used in proposed design.

CMOS is a term of performance limit which are specified the potential applications are identified with efficiency electronic properties along with physical modeling. On for constructing IC. In 10 stages delay line we are using 10 NOT gates to make a delay line with NMOS and PMOS to make CMOS transistor [1]. It is use 20 transistors and in 10 stage CMOS delay line. In the CMOS delay line the semiconductor material used that is silicon material. By using of this material and performance of various type of parameters such as voltage, leakage power, leakage current and propagation delay can be enhanced up to a limit [2]. It is found that reducing those parameters like as leakage current and power is major issue in present days.CNTFET is one possible solution to replacement CMOS-based integrated circuit technology, as the performance increase of conventional transistors witnessed during the last decades will arrive at its ultimate limits in the coming future [3].

Its present progress is largely dominated by the materials sciencecommunity due to many still existing materials-related obstacles for realizing practically competitive transistors. Compared to grapheme, carbon nanotube provides better properties for building field-effect transistors, and thus, has higher chances for eventually becoming a production technology. So, in this work it is used carbon nanotube field effect transistor in place of silicon based transistor [4]. Basically leakage current and power is the power and current when circuit is in switch off condition. In CNT technique we are using Carbon Nano Tube in place of silicon type semiconductor [5]. By using CNT leakage current, leakage power and propagation delay can be magnify and performance of circuit can be enhanced. In this article it has been proved that CNT transistor is a better replacement of CMOS transistor [8].

II. LITERATURE

CMOS based delay line:-

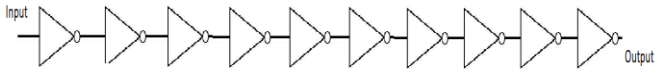

Fig 1:- 10 stage delay line

It is a delay line using 10 not gate. In figure1 all NOT gate connecting in series and give same output with some required propagation delay.

The design conditions of these delay factors are also discussed and correlated for the universal delay line circuits. As a conclusion, the main discovering of this article are focused and discussing the different and most efficient high-resolution delay line techniques [6].

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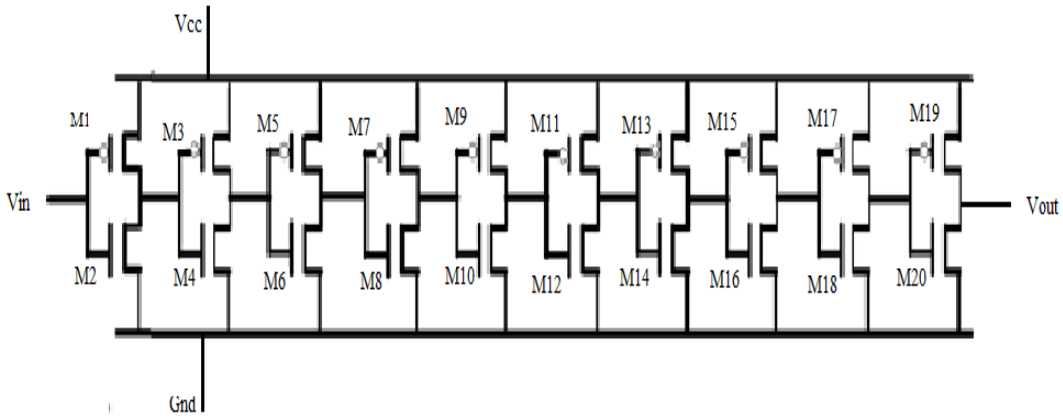

Fig 2:- 10 Stage CMOS delay line

It is represents the 10 stage CMOS based delay line at transistor level.In this figure 2 there are 10 inverter connected in series connection and current flow through the input is Vin. Input passing through those 10 inverter stages connected in series connection and then output found at output node thrown in figure 2 at Vout is similar as input but has some propagation delay. As It is a 10 stage delay line, so user can use 10 different delay values at individual output stage of each invertor output node. That's why this circuit is known as 10 stage invertor delay line.

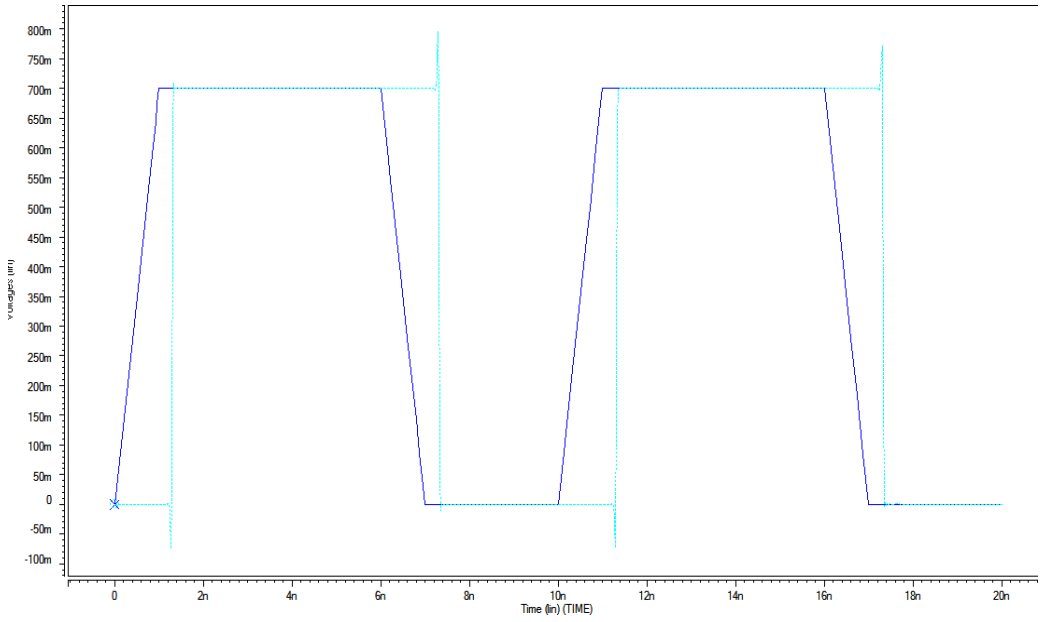

Fig 3:- Simulated waveform of 10 stage CMOS delay line

Parameters	10 stage CMOS delay line
Leakage current	10.5274e-12Amp
Leakage power	9.3692e-12Watt
Average power	4.1258e-08Watt
Propagation Delay	5.2016e-008Sec

Table 1. CMOS delay line simulation result

Here create a CMOS based delay line diagram,With a 10 NMOS and 10 PMOS transistor shown in figure2. Figure 3 shown the output waveform of 10 stage delay line. Now display in figure 3 it is clear that output will has same shape as input but with some required delay. Performance parameters of that delay line are given in table 1 with simulated results.

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III. PROPOSED CIRCUIT

10 Stage CNT delay line:-

In this article we have worked on CNT based delay line in which silicon based CMOS semiconductor replace by Carbon. By using this technique we can reduce leakage current and power. Carbon has many preferences over silicon semiconductor material. It has high tensile strength as comparison to silicon. It has high electrical conductivity in comparison to silicon. It also has big thermal conductivity and it is good electron field ammeters and many more. Because of these properties in this article silicon material is replaced by carbon.

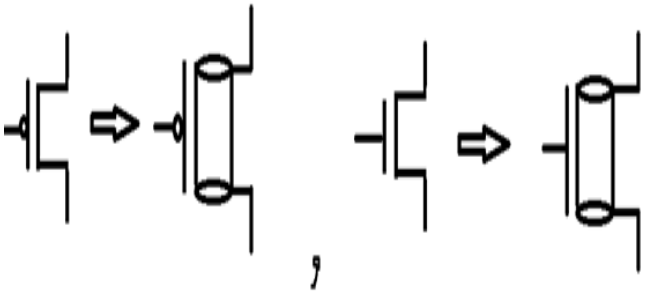

Fig 4:- Converting CMOS to CNT

The symbols of CNTFET are shown in figure 4.

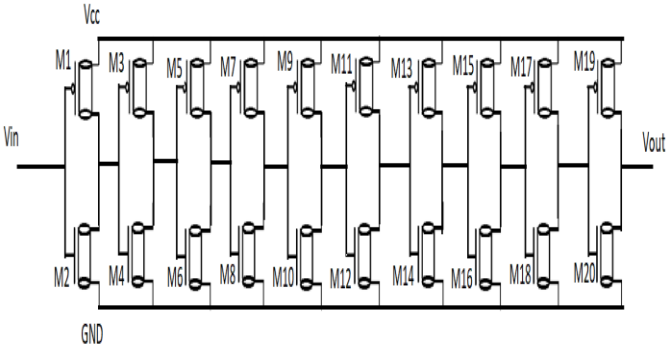

Fig 5:- 10 Stage CNT delay line

Here we represent a 10 stage CNT based delay line display in figure 5. In this figure 5 there are 10 inverter connected with series connection, 20 CNT transistors are used and voltage given at the input is Vin. Simulated waveform of proposed circuit (figure 5) is display in figure

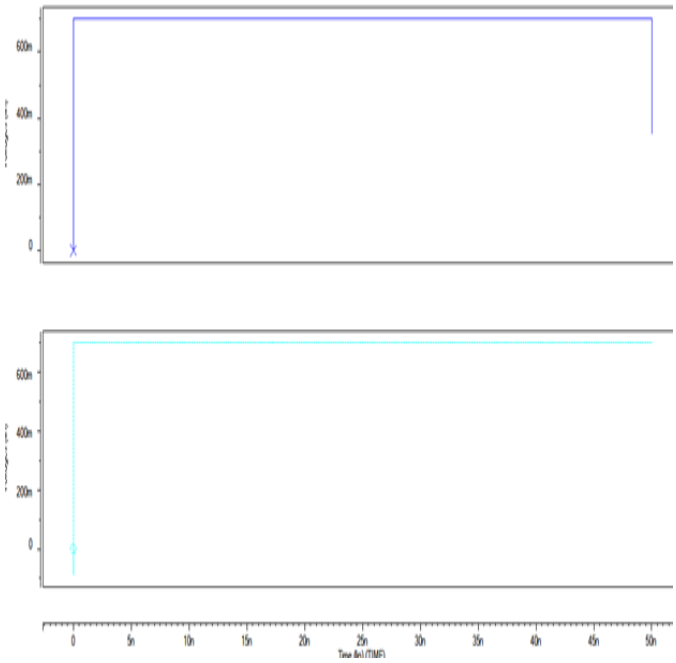

Fig 6:- Simulated waveform of 10 stage CNT delay line

IV. RESULTS COMPARISON

Parameters	10 stage CMOS delay line	10 stage CNT delay line
Leakage Current	10.5274e-12Amp	9.000e-13Amp
Leakage Power	9.3692e-12Watt	8.100e-13Watt
Average Power	4.1258e-08Watt	3.2594e-08Watt
Propagation Delay	5.2016e-008Sec	4.99e-008Sec

Table 2. CMOS delay line simulated result compared with CNT delay line simulated result.

10 stage CMOS and CNT delay line are simulated with the help of SPICE tool. After simulation it is found that leakage current in CMOS 10 stage delay line is 10.5274A and in the CNT 10 stage delay line it is 9.000e-13A, leakage power of CMOS 10 stage delay line is 9.3692W and in the CNT 10 stage delay line is 8.100e-13W, average power consume in CMOS 10 stage delay line is 4.1258e-08W and in the CNT 10 stage delay line is 3.2594e-08W and propagation delay found in CMOS 10 stage delay line is 5.2016e-008s and in the CNT 10 stage delay line is 4.99e-008s.

V. CONCLUSION

CNT transistors have many advantages over silicon transistor. It has been also verified in this article that the performance parameters like leakage current, leakage power, propagation delay and avg. power of CNT 10 stage delay line

have improved value then the CMOS based 10 stage delay line. For further improvements in results we can use various leakage rebate techniques like MTCMOS, SVL, AVL, LECTOR etc. It is also possible to reduce transistor stage for more improvements in results.

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