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An Ultra Low Power 5 – Phase Ring Oscillator using Lector Technique

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Abstract:- In this current article 5- stage ring oscillator designed with lector technique for reduction in leakage power without increasing the propagation delay. a lector technique to used two LCT transistor in which one of p-type and another one is n-type at each stage of ring oscillator and LCT is manage by source of second LCT transistor. In this current article is simulate and compare the various parameter are power dissipation, frequency, average power of 5- stage ring oscillator based CMOS as well as CNT at 32nm transistor based technology with the help of lector technique then comparison CNT based transistor better result display as compare to the CMOS based transistor using SPICE simulation tools.

Keywords:- *CMOS, carbon nano tube (CNT), lector, leakage power, leakage current.*

I. INTRODUCTION

From the former two decades the electronic industries have acquired an exceptional excellent growth. This rapid change in the market exists because of the quick and the rapid advancement in the technologies which are integrated because of the VLSI advent. In the current scenario the market has been captured via wireless devices being computers, GPS, cell phone, Wi-Fi, Bluetooth etc. these aforementioned devices are compact and they also make the wireless data available to other devices. There are certain frequencies which are to be worked upon for the transmittance and the receiving of the data [1]. There is a common circuit which is being used as a key for the modern communication is VCO. In any of the RF transceivers, CMOS VCO which is integrated completely exhibits a significant block. The main function of an oscillator is generating an analog and periodic signal whose frequency is stable and predictable. The output frequency provides AC waveform depends over the input voltage. A controllable frequency from a clock is generated by VCO. In this circuits to be used phase locked loop for the generation of clock VCO [2].

Regarding the ring oscillators, there are several applications of oscillators which form the vital building blocks in the circuits of RF and various mixed signals. The targeted field of applications varies along with the frequency of oscillators. It ranges and varies from Hz to MHz. Like all those oscillators pursuing high frequencies are utilized in phase locked loops, cyclotrons etc and there are various oscillators pursuing low frequency are utilized in radio communications, musical instruments etc. which are especially designed [3]. They can be made from the cascaded stages of inverter along with the LC tank circuits which depends over the frequency range which is essential and required. The main function of a conventional ring oscillator is producing oscillations varying from MHz range of frequency oscillation can be changed by adding stages number to it. Although the adding number of levels affects the oscillation frequency as enhancing the number of levels increases the circuit's propagation delay [4]. The practical acceptance of the addition of stages beyond 9 is negligible as the dissipation of the power is enhanced in the circuits and if the oscillations are being added in several hundreds of inverter stages then the oscillations of the frequency obtained is low whose further application is impractical and its fabrication and designing is not possible [5]. The best future nano-electric circuit is CNTFET circuit. This is the best and possible transistor for the future purposes. The conventional technology of CMOS approaches its physical limits which are fundamental whilst the downscaling as reported by Moore's law for the digital electronic is performed and done by CNTFET. In today's world as the significance and the consequence of the system-on-chips is increased therefore for the verification of the digital circuit performance, the only parameter to verify and check it should not only be the digital performance. CNTFET functions over transistor which is based on single carbon. This CNTFET was first introduced in 1998, since then there have been disparate alterations and changes done in it and if counted or developed according to the Moore's law each year the transistor should be double [6].

II. LITERATURE REVIEW

Mahani et.al (2017) reported a new fault tolerant delay cell for ring oscillators. In the phased and delayed locked loop and the clock data recovery, RO is considered as better crucial blocks, if discovered at faults they should be stuck for harsh environments and shouldn't be tolerated against SET (single event transient).). Hybrid tolerant fault topology to be design of delay cell whose is dependent and based over the role of sensitivity of each transistor. The mixture of three and four transistors redundancy forms hybrid tolerant fault topology. The software used by them is Cadence; their simulation results exhibit the fault tolerant delay cell dissipation of 34.34 µW power occupying the chip area of 127.2 µm2. This technology which was proposed by them exhibited decrease in the power consumption when compared to the current fault tolerant delay cells. Simultaneously, they depicted more reliability against

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single and multiple stuck faults along with SETs. If this proposed reliable delay cell was used in the ring oscillators, the acquired dissipation of power and the phase noise were about 249 µW and -96dBc/Hz respectively. Their higher reliability was to be acquired when they were compared to non-redundant ring oscillators [9].

Wu et.al (2017) stated the design ring oscillator which was applied using a pseudo-CMOS inverter; this was realized by n type transistors. They compared 11 stages using the conventional as well as proposed ring oscillator but both of them were fabricated by thin film metal oxide transistors comprising of the structure of etch stop layer. The results and the investigations depicted the delay product of power more than 50% by the proposed technology using the same supply voltage value. Oscillation frequency is increased the consumption of the power is reduced by 18% over the similar oscillation frequency. At the supply voltage a full swing can be received by acme voltage using their proposed ring oscillators [10].

Dhakad et.al (2017) stated VCO design in which the technique used was injection locking. The software used through which all the simulations were performed was Virtuoso Cadence Analog Design Environment using the SCL 180 nm CMOS process. The simulation results exhibited 150% tuning range was achieved by VCO over the range of 508 MHz to 3.56 GHz with phase noise of -126 dBc/Hz at 1 MHz offset frequency. When the voltage supply was 1.8V then the dissipation of the power of the circuit as an output was obtained to be 110.4µW [11].

Balaji et.al (2016) reported a novel method for designing low frequency CMOS ring oscillator producing the range of 1 Hz. The oscillator is designed in such a way that it comprises of structure of CMOS thyristor which was designed with the current mirror producing low frequency oscillations attaining less space of device comparing to conventional N stage ring oscillators. To achieve oscillations to the desired aspect ratios as well as the device parameters are designed with 90 nm technology. For analyzing the oscillator performance they investigated variation effect of voltage and temperature over frequency and the results of the simulations are exhibited [8].

Hanchate (2004) reported the enhancement of the leakage current sub-threshold along with increase in power dissipation to be statics which takes place due to the decrease in the threshold voltage because of the scaling of the voltage in the CMOS circuits. They proposed a LECTOR technique for CMOS gates designing, as these gates without enhancing the dynamic power consumption to be decreases leakage current. In their technique they have introduced two LCT transistors within the reach of the logic gates. In these logic gates the terminal of the gate of each control transistor is not controlled by itself they are controlled by the other sources. The arrangement is made in such a way that one of the LCT is always “near its cutoff voltage” regarding the combinations of input. The path resistance is increased to ground and therefore the leakage current is decreased. First net-listing to the gate level is converted to complex gate implementation in the given CMOS circuit, after this the introduction of the LCTs take place to attain a circuit which is leakage controlled. The importance of LECTOR technique is that it efficiently works in active as well as idle circuit state and when the results are compared they found that the leakage reduction was better in LECTOR than other techniques. The limitations which were exhibited by several other existing methods regarding the reduction of leakage were overcome by their proposed method. The average leakage reduction found in their experimental results were 79.4% in MCNC benchmarks circuits [7].

III. RESEARCH METHODOLOGY

In the family of oscillator, a ring oscillator circuit is a simple way of scheme to reducing power dissipation. Ring oscillator also called the relaxation oscillator so that the old number of inverter are connected in series connection and to obtain a natural oscillation as shown in a figure (1) CMOS based transistor to be used for design 5 stage ring oscillator. In this circuit input of first inverter are connected to the output of final inverter. Therefore the name of this circuit is ring oscillator.

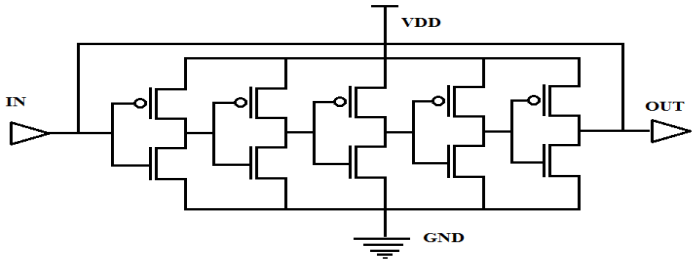

Fig 1:- 5- stage ring oscillator with CMOS technology

Now design 5- stage ring oscillator with carbon nanotube transistor based technology because CNT reduce leakage power due to smaller and shorter channel length and CNT made of rolded sheet of grapheme so that it is like a cylindrical shape as showing in a figure (2).

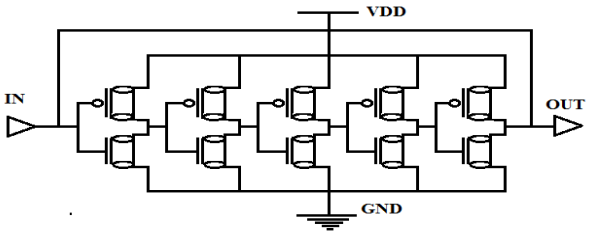

Fig 2:- five stage ring oscillator with CNT technology

Lector technique to apply in CMOS based 5 stage ring oscillator as showing in a figure (3). In this circuit (a) is the

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input/output node, five inverter is connected in parallel at each inverter has made of one PMOS and other one NMOS transistor in that circuit.

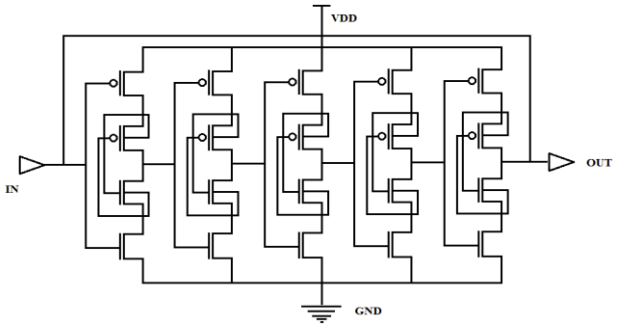

Fig 3:- 5 stage ring oscillator design with CMOS technology with lector technique

In the control box, Leakage controlled transistor (LCT) is attached in series connection of each five inverter M2 (PMOS) and M3 (NMOS) which are LCT. Leakage controlled transistor are join among pull up and pull down network. Gate terminal M2 is connect to the source of M3 and gate M3 is connect to the source M2. Similarly design CNT transistor based ring oscillator operates lector technique as showing in a figure (4).

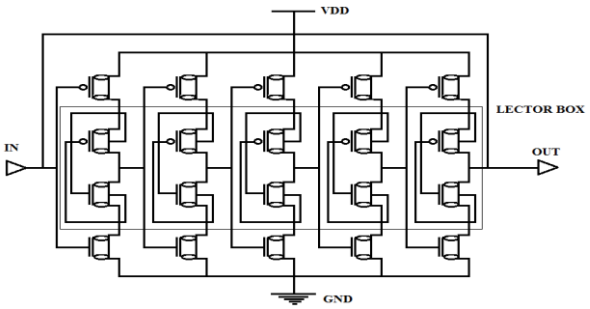

Fig 4:- CNT transistor based ring oscillator circuit applying lector technique

IV. SIMULATION AND RESULT

The proposed design is simulated using spice tool at 32nm. The length and width are taken as L=32nm and W=32nm at 1V supply is applied. First of all 5-stage ring oscillator is simulation with CMOS and CNT technology. Then second rig oscillator simulates with lector CMOS and lector CNT. The transient retaliation of lector CMOS are captured in the figure (5).

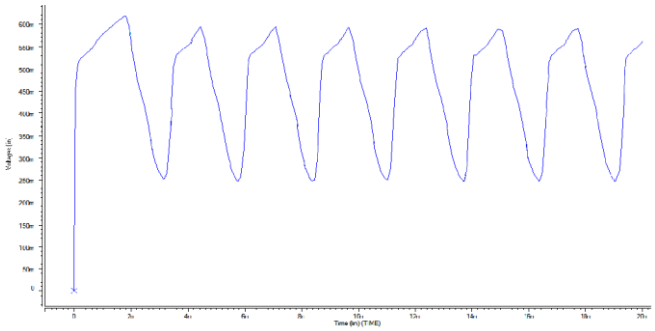

Fig 5:- Transient retaliation of lector CMOS

Now transient retaliation of lector CNT is captured in the figure (6). The transient retaliation of CMOS lector is simulated using the spice tools with 32nm channel length at 1V and the transient

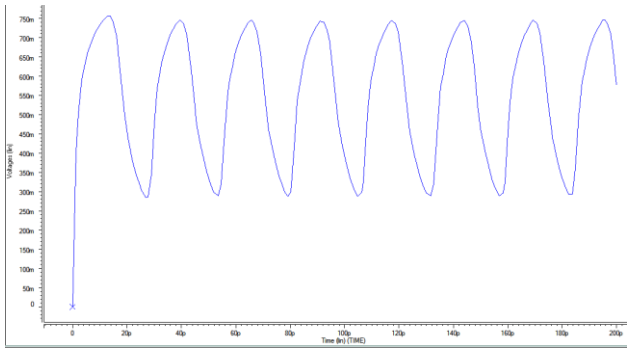

Fig 6:- Transient analysis of lector CNT

response of CMOS and CNT without lector technique generates oscillation frequency to 335MHz to 365MHz with 110% truing where as the transient response of CMOS and CNT with lector technique is simulated using spice tools with 32nm channel length at 1V then transient response of CMOS and CNT with lector technique is generate more oscillation frequency to 335MHz to 365MHz with 160% turning and the number of oscillation is more than the CMOS and CNT with lector technique.

Performance parameter	CMOS	CNT	LECTOR CMOS	LECTOR CNT
Technology	32nm	32nm	32nm	32nm
Supply voltage	1V	1V	1V	1V
Frequency	300MHz	340MHz	335MHz	365MHz
Leakage power	29.01E-10W	5.579E-10W	1.517E-10W	6.085E-05W
Leakage current	29.01E-10A	5.579E-10A	1.517E-10A	6.085E-05A

Table 1:- comparison with CMOS, CNT, lector CMOS, and lector CNT with spice tools.

The result are simulated of proposed circuit with pervious work are shown in table (1). In this table determine the four parameter using spice tools with 32nm such as leakage power, leakage current, frequency, average power at 1V.

V. CONCLUSION

A 5- stage ring oscillator was successfully designed and simulated using spice tools at 32nm channel length. The main target of this paper is to be reduced the power dissipation and leakage power. We create the previous paper work by reducing voltage and using CNT technology and the result in the table (1) presently comparison between CMOS and CNT. According to the acquired simulation results we judge that the proposed 5- stage ring oscillator with lector technique perform better result in the term of power dissipation and leakage current is reduce 23% at 1V. thus this lector technique to control leakage power for the circuit designers.

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