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Design of Efficient Serial Divider Using HAN CARLSON Adder

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Abstract:- Important block of a central processing unit in any computing system is Arithmetic and Logic Unit (ALU). Among all the arithmetic operations, division is considered to be more complicated and it completes after several cycles of time. Latency is increased because of the clock cycles. It is frequently utilized in the areas of signal and image processing applications. This work describes the architecture of a serial divider in combination with the influence of Han Carlson adder. Adder along with the non-restoring algorithm has been tested for the design of divider in the DADENCE platform. And found 48.67% reduction in delay over the existing method.

Keywords:- *Cadence, Han Carlson Adder, Serial divider, Non Restoring Algorithm, Delay.*

I. INTRODUCTION

Division operation is mainly used in scientific computation of image and digital signal processing. It can be accomplished either by serial division or parallel division. Serial division is slow when compared to parallel division but its structure is very simple. Parallel division is fast when compared to the former one but its structure is very complex. Division algorithm falls into two main categories, slow division and fast division, slow division includes restoring and non-restoring division, whereas fast division methods include Newton Raphson and Goldschmidt method of division [7].

In conventional method of processing, digital division operation performs subtracting the divider from a reference number, referred to as a current number which normally requires that the divider be added back to the current number depends on the result of the subtraction stage. In non-restoring method the selection of either addition or subtraction is carried out in the next computation stage [7]. Hence, the implementation of above requirement needs not only logic it also needs large circuitry. Due to the above this a pretty good amount of logic and related circuitry are required to implement restoring and non-restoring division algorithms. Digital recurrence is the simple and widely implemented class of division algorithm. The most common implementation of digit recurrence division in modern microprocessors is division from the initials of Sweeney (S), Robertson (R) and Tocher (T) named SRT, who developed the algorithm independently at approximately the same time. SRT division uses subtraction as the fundamental operator in order to have a fixed number of quotient bits in each iteration. Intel Pentium-4 Processor makes use of SRT division [1] and [6]. Division operation consumes more time when compared to addition, subtraction and multiplication [2] and [3]. Fast division method can be used but there is complexity in the structure when compared to the slow division. Thus an efficient algorithm which can improve the efficiency should be followed.

II. TYPES OF EXISTING DIVISION ALGORITHMS

Many algorithms used for serial division. Decimal division uses the traditional method which done normally i.e. the use of pencil and paper method [6]. The iterative process of the subtraction and shifting operation is carried out for certain steps and hence called digit recurrence division algorithm [6]. In the digit recurrence algorithm, single iteration calculates one bit of the quotient. Partial remainder which is obtained by shifting is compared with multiples of the divisor for determining quotient bit. The control unit of this recurrence algorithm contains the Adder/subtractor modules which makes implementation of the algorithm easy and high level of accuracy. There occurs cerain disadvantage like more timing complexity due to this algorithm, when compared with multiplicative division algorithm [4] and [6].

There are three types of digit recurrence algorithm like restoring, non- restoring and SRT [6]. For multiplicative type of division algorithm, iteration is functional which uses convergence techniques, starting from initial estimation till the determination of quotient with required accuracy and SRT is used. This algorithm leads to high performance when compared to the existing recurrence division algorithm. The demerits of this algorithm are that it has complex steps and it requires more number of computations required to get the final remainder. This type of division is possibly seen in commercial applications like microprocessors and mainframe computers [3] and [4]. Another method which is also a functional iteration based algorithm is called Newton-Raphson method. Gold Schimdt's algorithm is the another algorithm for functional iteration where both numerator and denominator are multiplied with the same number and thus the fractional value remains same.

III. NON RESTORING SERIAL DIVISION ALGORITHM

Digit recurrence algorithm is the most common algorithm though there were many literatures about several division algorithms. This algorithm is again divided into SRT type [6], restoring and non-restoring algorithm. The Digit is the basic algorithm in which a non-restoring algorithm is used to design a digital serial divider. Generally recurrence algorithm mentioned above makes use of iterative addition, subtraction and shifting operations in order to perform the division process. Division based on digital serial approach is simple and cheap whereas parallel digital division approach has high costly and increased complexity. Digital serial division is much slower when compared to parallel approach. But the design of hardware is complex and also parallel approach is expensive which serves to be a tradeoff while choosing either serial approach or digital parallel type of division [4].

The digital serial division architecture based on the non-restoring type of division technique is used. For this particular digital design, the required remainder and corresponding quotients in non-restoring type of division is found by using the iterative process of add/subtract and shift [4]. Here the adder cell used is Han Carlson adder. The adder cell is controlled by quotient determined in the previous step in order to perform the addition or subtraction. With the help of shift register, the partial remainder is shifted to get the required output.

IV. EXISTING SYSTEM

Ripple carry adder (RCA) is used in the existing serial division technique. RCA is the simplest type of adder [2]. It consists of series of full adder till 'n' bits. RCA architecture is simple to design and for more number of bits processing this simple structure may take some time period to process. The delay can be reduced if the structure of the RCA is modified in the existing adder. By keeping this into consideration the methods have been proposed for adders. One of the suitable addition methods for the divider is Han Carlson adder.

V. IMPLEMENTATION OF PROPOSED SYSTEM

Han Carlson adder along with non-restoring technique is used in the proposed design of serial divider. It also functions with the parallel prefix adder concept [1]. It has black cells, gray cells and buffer. Black cell is the combination of one OR gate and two AND gate. White cell is the combination of OR and AND gate. Buffer gives output value same as input value. Whereas it differs from other adder and it can be utilized for large word sizes. On comparing with other adders Han Carlson has low latency [5]. VerilogHDL coding for the above logic has been done and has also been tested by using CADENCE platform. The structure of Han Carlson adder is shown in fig.1.

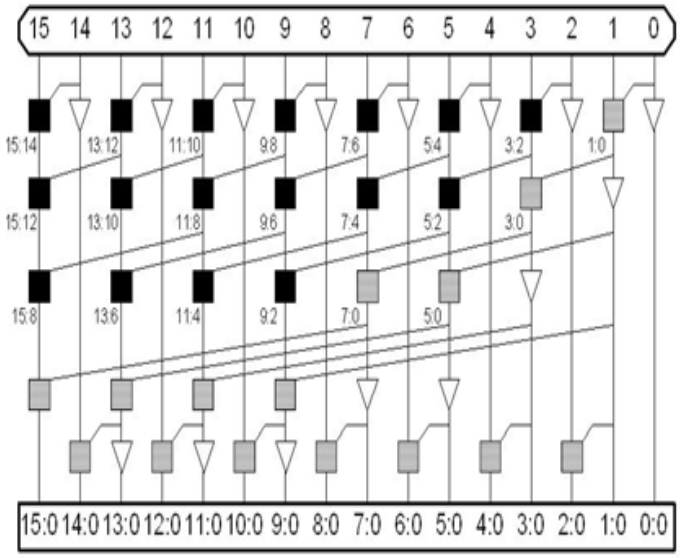

Fig 1:- Structure of Han Carlson Adder

The architecture of serial division is implemented using a 16-bit adder and subtractor unit. The adder and subtractor unit are the first and important blocks of serial divider. Its operation has been verified by giving suitable inputs.

VI. EXPERIMENTAL RESULTS

Comparison of existing serial divider module and proposed module in terms of delay is given in Table 1.

Delay of Existing System	55.28ns
Delay of Proposed System	26.904ns

Table 1:- Comparison of Proposed System

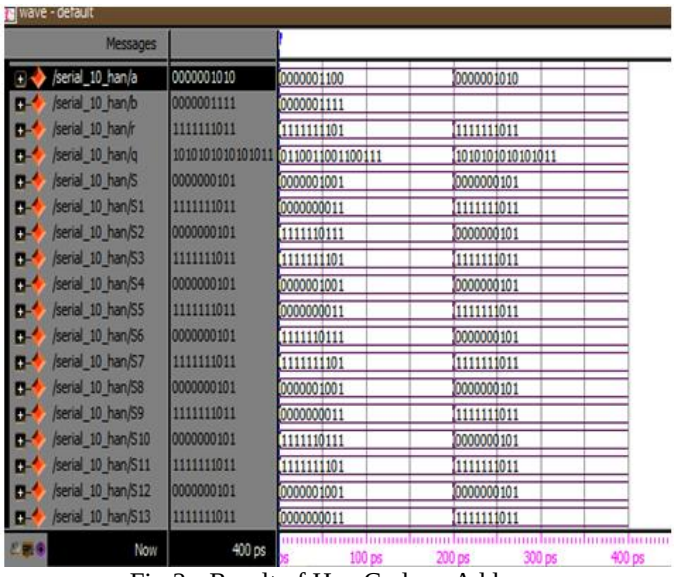

Fig 2:- Result of Han Carlson Adder

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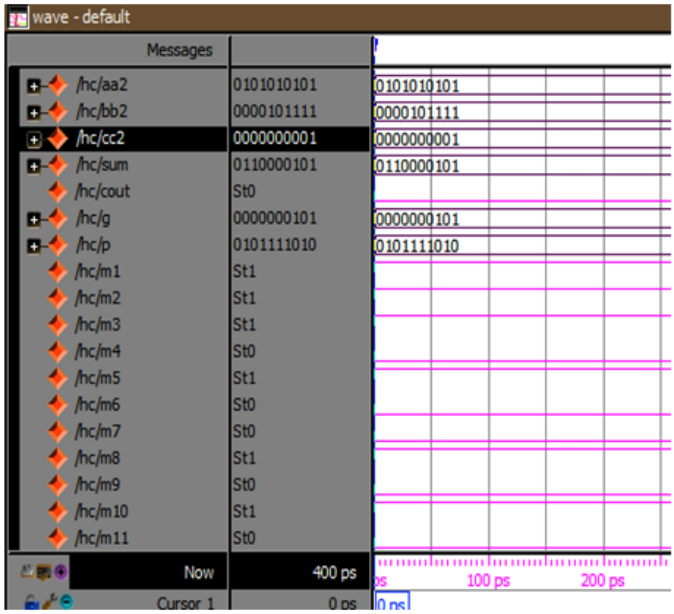

Fig.3: Result of Proposed Divider

The simulated results have been given in Fig.2 and Fig .3 for Han-Carlson and the Proposed Divider respectively.

VII. CONCLUSIONS

Arithmetic divider is the primary block of image and signal processing applications. The proposed divider system featured with Han Carlson adder and Non- Restoring algorithm has been tested for many examples and found satisfactory results with the delay reduction of 26.904 ns which is 48.67% improvement in delay efficiency of the proposed system over the existing system. Results have been tested by using CADENCE platform.

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