ISSN No:-2456-2165

A Review of Binary to Gray and Gray to Binary Code Conversion

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Abstract:- In today's world of electronics industries low power has emerged as a principal theme. Power dissipation has become an essential consideration as area for VLSI Chip design and performance. With shrinking technology reducing overall power management and power consumption on chip are the main challenges below 100nm as a result of increased complexity. When it comes to many designs available, power optimization is essential as timing as a result to the demand to extend the battery life and reduce package cost. Asto reduce the power consumption we have many techniques from those techniques, lets we implement on Reverse Logic. In reversible logic it as greater advantage and executing in high speed, with less power dissipation which is implemented by using basic logic gates in less area. For data security, decreasing the arithmetic operations complexity hence reduced requirement for the device hardware, reducing the switching activity level resulting to power saving and increased speed among other factors which is widely done by using code conversion in digital system, therefore, In this paper, reviewing to papers which are based on Binary to Gray and Gray to Binary Code Conversion.

I. INTRODUCTION

Reduction of power consumption is one of the main objectives in modern circuit design. In early 1960s, R. Landauer demonstrated that irreversible hardware computation despite its realization method, leads in energy dissipation as a result of data loss. However, the reversible logic circuits have theoretically zero internal power dissipation because there is no data loss. Therefore, Bennett in 1973 demonstrated that to avoid KTIn2 joules of energy dissipation in any circuit, reversible logic gates must be included in the circuits.

If the input vector can be uniquely recovered from the output vector, and there is a one-to-one corresponds between its output and input assignments, then the circuit is said to be reversible not only the inputs can be recovered from the outputs but also the outputs can be uniquely determined from the inputs. This research clearly presents a design of reversible code converters includes reversible excess3 to BCD code converter, reversible BCD to excess 3 code converter, reversible gray to binary converter, and reversible binary to gray code converter.

II. LITERATURE REVIEW

One of the promising computing technologies assuring zero power dissipation is the Reversible Logic. Reversible Logic has a wide spectrum of applications like Nanotechnology based systems, Bio Informatics optical Circuits, quantum computing, and Low Power VLSI. Therefore, this paper represents the 4 bit reversible comparator based on classical logic circuit which uses existing reversible gates. The design simply aims at reducing optimization parameters like quantum cost, garbage outputs, and the number of constant inputs. The results obtained in this research work indicate that the proposed comparator has one constant input and 4 quantum cost less than the prior design [1].

With dynamism in technological generation, the field of nano meter technology results to reducing the power consumption of the logic circuits. One of the promising technologies gaining greater interest is the reversible logic design due to low power consumption and less dissipation. in the current technological world, digital systems code conversions is commonly used process for reasons such as reducing the complexity of arithmetic operations, enhancing data security hence decreasing hardware requirement and this automatically drops the switching activity level resulting to power saving and more speed of operations among other factors. Therefore, this research proposes the novel reversible logic design for code conversion such as Excess 3 to BCD code, BCD to Excess 3 code, Gray to Binary code, and Binary to Gray code [2].

Improvement in the field of nano meter technology results to reduced power consumption of the logic circuits. The logic design has been one of the promising technologies that are gaining more interest as a result of low power consumption and less dissipation. Besides, in this digital generation, the code converters are commonly used processes. Therefore, the reversible circuits and reversible logic gates for realizing the code converters like as Excess 3 to BCD codes, BCD to Excess 3 code, Gray to Binary code, Binary to Gray code using the reversible logic gates is proposed in this research work. It is a challenging task to design the reversible logic circuit since not adequate number of gates is present for the design. The reversible processor design requires needs its building blocks should be reversible in this manner for designing of the reversible code converters is one of the most important one. In this digital generation, information or data is represented by a combination of 1's and 0's. Therefore, it is important to note that a code is basically the pattern of these 1's and 0's used

to represent the information. Hence, a class of combinational digital circuits that are used to convert one type of code into another is known as the code converters and the proposed design results to decreased power consumption as compared to the conventional logic circuits [3].

However, the reversible rationale has pulled in individuals' consideration progressively due to its application in optical figuring, quantum processing, and low power CMOS outline. This research exhibits the novel outlines of a few reversible converters that are enhanced as far as steady data, refuse yield, and the quantum expense. Therefore, the improved outline of the reversible converters exhibited in this research are reversible Excess-3 to BCD converter, reversible BCD to Abundance 3 converter, reversible Gray to Binary converter, Binary to Gray converter, and the reversible Aiken to BCD converter [4].

In today world of electronics industries, low power has emerged as a principal theme. Therefore, power dissipation has become an essential consideration as area for VLSI Chip design and performance. With the shrinking technology decreasing over all power management on chip and power consumption are the main challenges below 100nm as a result to increased complexity in general. When it comes to many designs in today's world, power optimization in essential as timing as a result to the requirement to extend the battery life and reduce the package cost. As to reduce the power consumption we have many techniques from those techniques, lets we implement on Reverse Logic. In reversible logic it as greater advantage and executing in high speed, with less power dissipation which is implemented by using basic logic gates in less area. For data security, decreasing the arithmetic operations complexity and thereby dropping the level of switching activity resulting to power saving and more speed, reducing the general hardware requirements among others which is commonly done by application of the code conversion in the digital system which is widely done by using code conversion in digital system. therefore, this research work deals with Excess 3 to BCD code, BCD to Excess 3 code, Gray to binary code, Binary to gray by utilizing the reverse logic gate [5].

Current applications of quantum computing are the evaluations and design on the reversible logic technology. Many systems assembled in this digital generation commonly use the code conversion technology in minimizing hardware requirement and enhancing the data security. The nano-metric technology is high prolific in the current digital systems since it reduces power consumption in the logic circuits. Therefore, this research work simply proposes the reversible logic design for such a code conversation entailing excess 3 to BCD code, BCD to excess 3 codes, gray to binary code, and the binary to gray code [6].

In the field of quantum computation, the nanotechnology and the reversible logic has obtained a lot of attention of researcher's in the current years a s a result of its low power dissipation quality. Therefore, the quantum computing has been a guiding principal for low power VLSI, DNA computing, low power CMOS design, optical information computing, nanotechnology and bio-informatics. In digital system, Code converters are considered to be very essential component and are needed day in and out. Generally, the encoders are utilized in converting a 2n bit number to n bit number. In this paper, an optimized design of Decimal to BCD code converter using a new proposed reversible gate i.e. FR gate is proposed. The proposed design offers an improvement of 26.67% and 54% over the existing design in terms of its garbage outputs & Quantum cost respectively. The Proposed gate and Decimal to BCD converter are finally designed& successfully tested using the simulations obtained from QCA designer [7].

One of the latest technologies having promising applications in quantum computing is the reversible logic. The reversible code converters are a class of the reversible circuits that are applied to convert one type of code into another type of code. Therefore, it is important to note that code conversion is commonly used process in much digital system to assist in reducing the hardware requirement, reducing the complexity of arithmetic operations, and enhancing data security. This research work presents the design of the reversible code converters for instance converting BCD to Gray code, Binary to Gray code, BCD to excess-3 code, and Binary to BCCD code. Majority of circuits have been designed and synthesized using the QC Viewer. Therefore, the circuits are evaluated in terms of number of quantum cost, garbage outputs, ancilla inputs, and the qubits [8].

The current VLSI technology is based on CMOS technology, and the development of the Very large Scale Integration technology has reached its peak as a result of the fundamental physical limits of the Complementary Metal oxide Semiconductor technology. The current challenges, as well as the physical limitation of the traditional CMOS technology have overcome by the QCA which was first introduced by C.S. Lent. Therefore, it is important to note that the nano scale size quantum cell is a feature of the Quantumdot Cellular Automata technology. Therefore, this research work proposes a new Quantumdot Cellular Automata (QCA) structure for 4bit gray to 4bit binary and 4bit binary to 4bit gray using the two input XOR gates. Besides, these structures are simulated and designed with the QCA designer and compared with the previous constructed structures [9].

In the current technological generation, the VLSI designers were mainly concerned with power minimization of the digital circuits. Therefore, the reversible logic design has emerged as one of the most powerful device as a result of its low power consumption feature that is not present in the previous devices. Additionally, the adiabatic logic is one of the solutions for minimization of energy in general. This research work presents both combined reversible and adiabatic logic. Additionally, for the ultra-low power circuits a modified positive feedback adiabatic logic (MPFAL) is presented in this paper whose DC voltage range is of 0.1 to 0.3V. It is a dual rail and diode-free logic which offers both true and complementary outputs. In the proposed research, Binary to Excess-1, Gray to Binary, and Binary to gray converters are designed using MPFAL and PFAL

adiabatic logic methods and are compared with the conventional CMOS. Therefore, the designed circuits are simulated on Mentor Graphics device using the TSMC 180nm technology node. Additionally, the simulation results show that the designed circuits achieves power saving in the range of 74-23% at the frequency range of 0.1-100 MHZ [10].

One of the most promising research areas in the past few decades and has found its usage in many technologies is the reversible logic such as optical computing, nanotechnology, and low power CMOS. Therefore, the main role of designing reversible logic is simply to reduce the number of garbage outputs, depth of the circuits, and quantum cost. The idea behind this research is to give an understanding and overview of the reversible gates and a frame of reference regarding the reversible gates. Therefore, this research presents various logic gates and their application on logic design has been widely discussed. Additionally, a brief framework of comparisons between several reversible circuits presented on the basis of many parameters [11].

III. CONCLUSION

In conclusion, this research work has introduced the review of reversible circuits and reversible logic gates for realizing different code converters like Gray to Binary, Binary to Gray, Excess-3 to BCD, and BCD to Excess-3 using reversible logic gates. Therefore, this research work leads to the introduction of the power consumption compared with the conventional logic circuits.

REFERENCES

[1]. Rakesh Kumar Jha1, Arjun singh yadav, "An FPGA Implementation of Energy Efficient Code Converters Using Reversible Logic Gates", in International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 5, Issue 1, January 2016.

[2]. M.Saravanan, Dr.K.Suresh Manic, "Energy Efficient Code Converters using Reversible Logic Gates", International Conference on Green High Performance Computing, 2013.

[3]. Ponnuru Koteswara Rao, P Raveendra, Kankata Venkateswara Rao, " Implementation of Effective Code Converters using Reversible Logic Gates", *Ponnuru Koteswara Rao. Int. Journal of Engineering Research and Applications, May 2016.*

[4]. Parikshit A.Awati, Vaishali Raut, "Design of Energy Efficient Code Converters using Reversible Logic Gates", International Journal of Innovations & Advancement in Computer Science, Volume 4, Issue 6 June 2015.

[5]. KOTHAPALLY NIKHILA, VENKATA CHARY, N. BHOJANNA, G. SUJATHA, "Optimized Reversible Logic Gate with Energy Efficient Code Converters", International Journal of VLSI System Design and Communication Systems Volume.02, IssueNo.06, September-2014, Pages: 0379-0383.

[6]. M.Saravanan, K.Suresh Manic, Umasuresh, Aravind CV and John Wiselin, "Design of Reversible Logic Gates for Digital Applications", Asian Journal of Electrical Sciences ISSN 2249 - 6297 Vol. 2 No. 1, 2013, pp.36-40.

[7]. Kunal Chaudhary 1, Gurpreet Kaur, "Design of Decimal to BCD Code Converter using Reversible logic and QCA", International Journal of Innovative Research in Science,Engineering and Technology, Vol. 5, Issue 9, September 2016.

[8]. Manjula Gandhi S, J Devishree, " Design of Reversible Code Converters for Quantum Computer based Systems", *Amrita International Conference of Women in Computing (AICWIC'13).*

[9]. Md. Tajul Islam, Golam Sarwar Jahan, Ali Newaz Bahar, Kawsar Ahmed, Md. Abdullah Al Shafi, "A new efficient non reversible 4 bit binary to gray and 4 bit gray to binary converter in QCA", NANOSYSTEMS: PHYSICS, CHEMISTRY, MATHEMATICS, 2018.

[10]. T. Durga Prasad, B.Anil Babu, "ENERGY EFFICIENT CODE CONVERTERS USING MODIFIED POSITIVE FEEDBACK ADIABATIC LOGIC", International Journal of Innovative Research in Engineering and Applied Sciences, August 2017.

[11]. Shefali Mamataj , Dibya Saha , Nahida Banu, "A Review of Reversible Gates and its Application in Logic Design", American Journal of Engineering Research (AJER) e-ISSN : 2320-0847 p-ISSN : 2320-0936 Volume-03, Issue-04, pp-151-161.