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Low Power Consumption Based Johnson Counter by Transistor Gating Technique

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Abstract:- Johnson counter is an important counter which is mainly used to deliver data of particular concept in a continuous loop. This method is essential for varying logic designs. Normally data that follows this pattern is placed inside a certain place that follows the same design and a perfect logic function is constructed. The presence of the counter system is an essential part of these logic designs since they provide a wide range of sequences. In the Present time , Every Digital circuit is going to short in Area. In this case , Power Consumption is a crucial Point. Johnson Counter is using in many Digital Circuits. In this paper, we are working for the Power Consumption of the 4 Bit Johnson Counter. For Reduce the Power Consumption , using Transistor Gating Technique. It will reduce the Power consumption of the NAND gate , D Flip Flop and PIPO Circuit. For Design the circuit, working at 130 nm Channel length file.

Keywords:- *CMOS, Counter, Flip-Flop, Johnson Counter, Sequential Circuit.*

I. INTRODUCTION

Johnson encounter is a method where the output received from the final shift register is inserted into the initial shift register in the form of a input. The data revolve around the ring in the form of binary digits. This type of method is also called as Mobius counter or twisted ring counter.

A. Ring Counter

In this method a circular shift register is used to send the data values. Similar to the previous one, here also the final output of one of the shift register is inserted into the initial shift register in their input slot. Due to the presence of the Hamming distance it prevents the occurrence repeat. The value is usually 2 in over beck counter and 1.

There are two types of ring counters:

- The first straight ring counter connect the out of one register to another one's input in an proper order from last to first in a circular motion. Either a 1 or 0 is shifted around continuously. Like in case of a 4-register one-hot counter, when a value like 1000 is inputed then they produce varying outputs like 0010, 0001, 1001…. For proper result a single binary data is a 1 or 0 should be added in advance.
- In case of Johnson counter the shift registers are connected in a circular motion, by connecting one output to others input. The data source are being flown continuously in a circular loop providing multiple results like when 4 register counter data of 0000 is inserted the result would be 0001, 0101,…

Johnson counters are the most commonly used methods since they provide multiple result from the same amount of shift register and they do not required the input of binary data for startup.

II. JOHNSON COUNTER (4 BIT)

Note the inversion of the Q signal from the last shift register before feeding back to the first D input, making this a Johnson counter.

- Enable the flips flops by clicking on the RESET (Green) switch. The RESET switch is an on/off switch (similar to a room light switch)
- Click on CLK (Red) switch and observe the changes in the outputs of the flip flops. The CLK switch is a momentary switch (similar to a doorbell switch - normally off).
- The D flip flop clock has a rising edge CLK input. For example, Q_1 behaves as follows:

✓ The D input value just before the CLK rising edge is noted (Q_0).

✓ When CLK rising edge occurs, Q_1 is assigned the previously noted D value (Q_0).

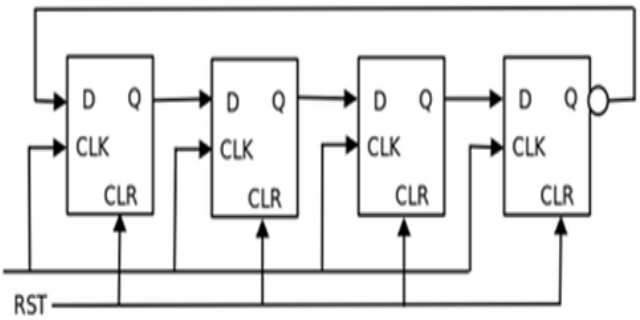

Fig 1:- Johnson counter

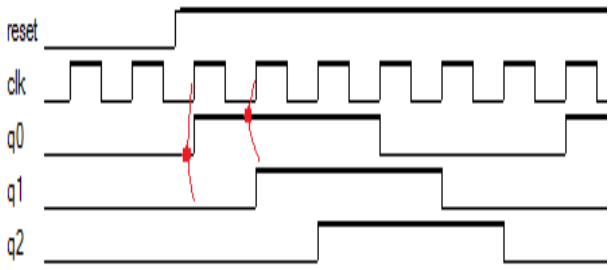

Fig 2:- Output Waveform for Johnson Counter

A. Applications

Certain logical designs like ASIC uses the ring counter Technology for providing efficient and hard state machines. most of the binary counters use adder, a circuit which is more difficult to deal with when compared to the ring counter technique. Also, show the propagation delay occurring in a adder circuit is equal to the number of bits available in the code. but in case of the ring counter, the delay is constant describe the number of bits used in the code. Also, Adder circuit causes several timing errors affecting the Hardware of the system while the ring counters with the hamming distance of 2 detect even a single problem happening in the system.

A 5-stage Johnson counter Is mainly used as a frequency divider and they are also used as signal generators. the signal generators are mainly used in certain digital systems that require perfect timing signals that synchronise with the central clock. the Johnson counters provide a flawless and 50% output for each cycle. Amann et al. [15] stated that with the help of FSM's The Johnson counters can store near 30 % of the product terms and produce the output. they are also used to drive stepper motor circuits.

III. LITERATURE REVIEW

Johnson counter Is one of the most famous and widely used technique that delivers a particular pattern of information within the loop up in particular intervals continuously for different logical designs. the current computer designing system I'm made fuse of this particular pattern where a data is sent in the form of fragments into a system for performing the particular function. also in order to establish this Logix, it is essential to input the data in a perfect interval of time I'm like a clock cycle. hence sequential circuits are the essential part of computer designs which is embedded in the chip of the computer. with the area of the chip reducing considerable e reliability has become a major issue while designing a computer circuit. Reliability like power dissipation is one of the most major issues while designing. one of the most common techniques that is used to reduce the amount of power dissipation is clock gating technique. With the help of this technique, unwanted clock pulses are being neglected and only the essential pulses are taken into account. continuous researches are being conducted to increase the application of this clock gating technique. crop transition is one of the major factors that creates power dissipation. nearly 15 to 45 percentage of dissipation it is mainly due to these clock transition problems.[1]. So, with the help of a perfect clock management system the problem of power dissipation can be easily prevented.

IV. D FLIP FLOP

Figure 3 is showing the circuit for the D Flip Flop by use NAND Gate. As we can see from the Figure 3.10 , using two inputs D and Clock while 2 output Q and Q_Bar. In this Design using 4 NAND Gate Design while one inverter is using. Set and Reset input bar will be Logic High. That means the value of these input will logic 1. Q and Q_bar are the outputs of the D Flip Flop.

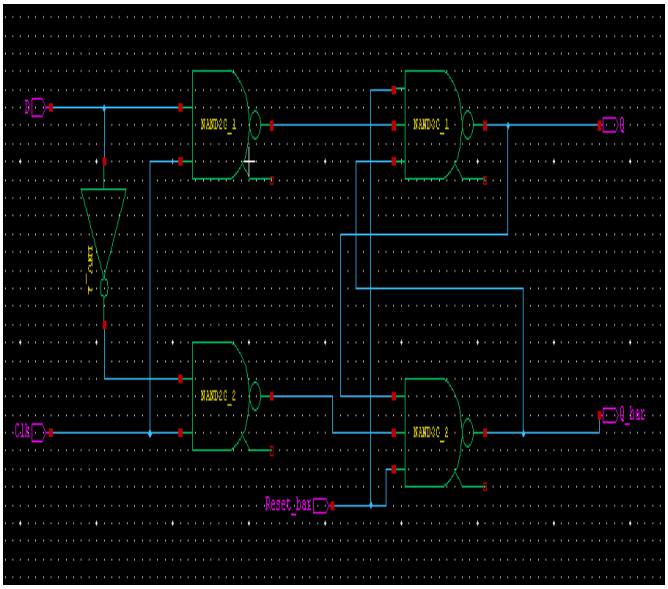

Fig 3:- D Flip Flop

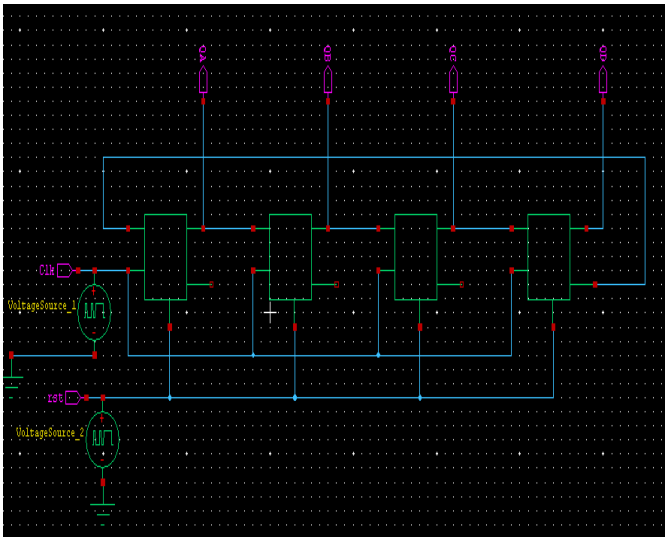

Fig 4:- Johnson Counter

Figure 4 is showing the circuit for the Johnson Counter by use D Flip Flop. As figure 4 is showing the input of the Johnson Counter are reset and Clock while output are A0, B0, C0 and D0. Set and Reset bar of every D Flip Flop will be High.

V. PROPOSED METHODOLOGY

A. Transistor Gating Technique

In this method, two sleep transistors are being used. One transistorsnsistor is placed between the pull-up network and the output of the circuit and another between the grouthe nd and pull-down network. the main these transistorsnsistor is to prevent the current leakage and completely using ahe the gating techniques.[2]. The Transistor Gating Technique is shown in Figure 5.

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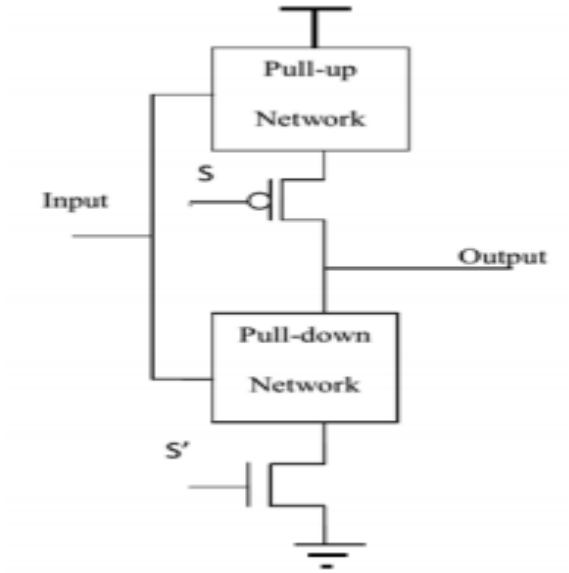

Fig 5:- Transistor gating technique

Figure 6 is showing the circuit for the NAND gate by use Transistor Gating Technique. As Figure is showing, two extra transistors have been added from Pull up network and Pull Down Network. These transistor will stop the Leakage power of the circuit. A PMOS transistor is connected by Pull Up

Network and a NMOS transistor is connected by Pull Down Network. The input of these transistor will be logic Low . That means input of these transistor will be logic 0.

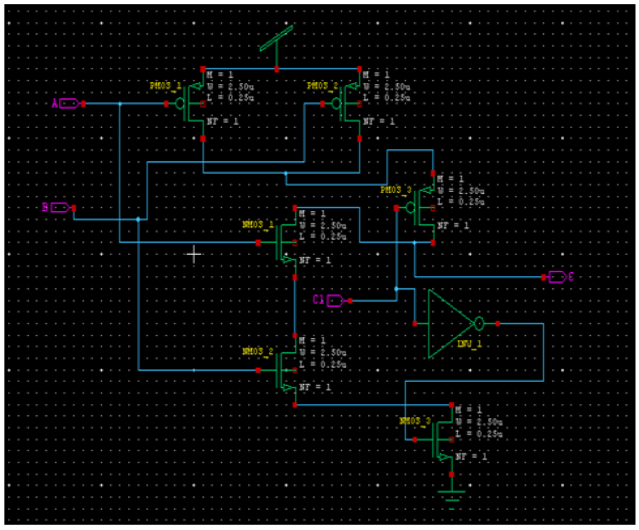

Fig 6:- Proposed NAND Gate

Figure 7 is showing D Flip Flop by use Transistor gating Technique. In this design , replace the 2 NAND Gate Circuit of the D flip flop by proposed NAND gate Circuit. Third input of the NAND gate will be Logic 0. In the Proposed D Flip Flop circuit only 2 NAND gate will replace. Next 2 NAND gate can't replace because these 2 NAND gates are changing the output waveform of the circuit.

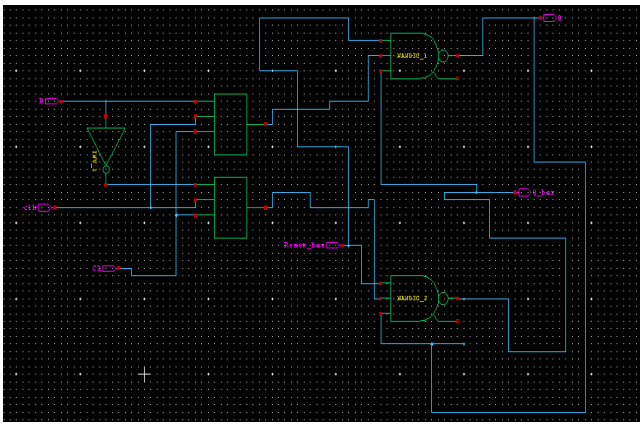

Fig 7:- Pro D Flip Flop

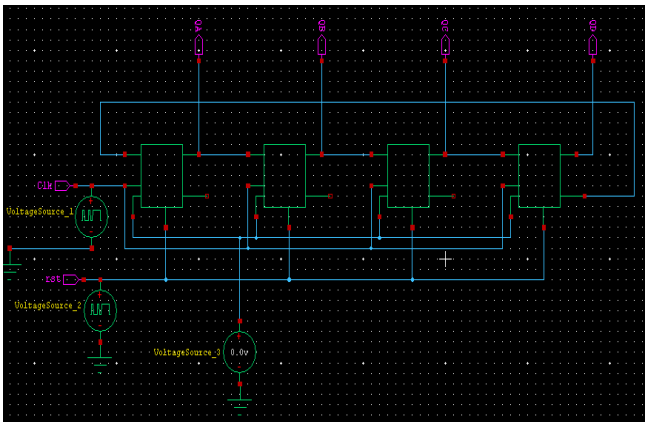

Fig 8:- Proposed Johnson Counter

Figure 8 is showing the Proposed Johnson Counter circuit by use of Transistor Gating Technique. In this Circuit , Transistor Gating Based D Flip Flop is using. That D Flip Flop is design by Transistor gating based NAND Gate.

VI. RESULTS

In this section, showing the results of the Existing Johnson Counter and Proposed Johnson Counter. In this Clock and reset are the inputs while QA,QB,QC and QD are the outputs. Power consumption for Existing Johnson Counter is 2.101739e-002 watts.

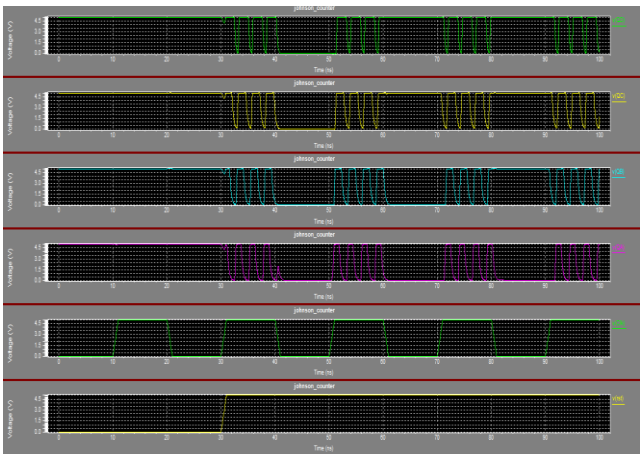

Fig 9:- Existing Johnson Counter

Fig 10 is showing the output waveform for proposed Johnson Counter. Power consumption for proposed Johnson Counter is 5.738886e-004 watts.

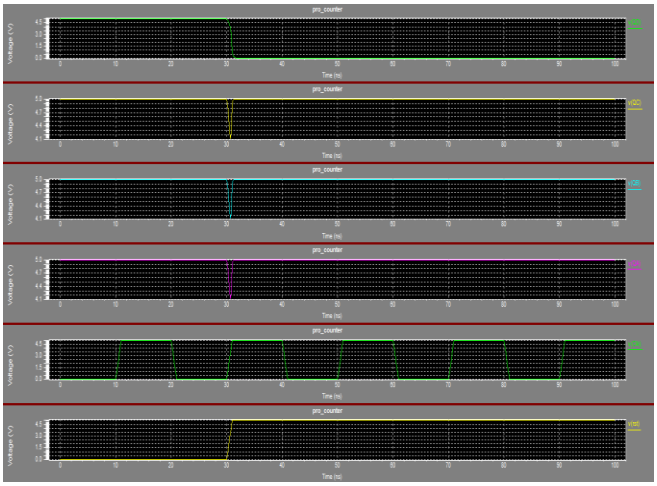

Fig 10:- Proposed Johnson Counter Waveform

	Power Consumption
Existing Johnson Counter	2.101739e-002 watts
Proposed Johnson Counter	5.738886e-004 watts

Table 1:- Comparison Table

VII. CONCLUSION

In this Research, reducing the Power Consumption of the Proposed Johnson Counter circuit. For Reduce the Power Consumption, using Transistor Gating Technique. It will reduce the Power consumption of the NAND gate, D Flip Flop and PIPO Circuit. For Design the circuit, working at 130 nm Channel length file. As Results are showing for the NAND gate , D Flip Flop and Proposed Johnson Counter Power Consumption is reducing from the Existing Circuit. Normal Johnson Counter circuit power consumption is 2.101739e-002 watts while proposed D Flip Flop circuit Power Consumption is 5.738886e-004 watts. That means Power Consumption is reducing for the Transistor gating technique.

FUTURE SCOPE

In the Future, we can further Reduce the Power Consumption of the circuit. In the Future ,we can work at Area also. We can reduce the Area of the circuit.

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