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Performance Analysis and Implementation of Cascaded H-Bridge Multilevel Inverter Fed Induction Motor Drive using TMS320f28335 DSP Processor

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Abstract:- Multilevel inverters are suitable for high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and reduced filter requirements. Three phase multilevel inverter fed induction motor drive is designed, employing Cascaded H-Bridge multilevel inverter. The inverter consists of series-connected half-bridge modules to generate the multilevel waveform and a simple H-bridge module, acting as a polarity generator. This topology, features many advantages when compared with the conventional multilevel inverters which include stability, simple control, reduced number of DC voltage sources and less devices count and also maintains a constant voltage at the output side irrespective of the load variations. The phase opposition disposition (POD) pulse-width modulation technique is employed to control the inverter. The inverter can then be connected to feed motor drives, which introduces a reduction in the THD of machine currents. The performance study of induction motor drive is carried out with MATLAB/SIMULINK. Hardware is implemented using TMS320F28335 digital signal processor.

Keywords:- *Multilevel Inverter, Control Schemes, Motor Drive.*

I. INTRODUCTION

Multilevel inverters are suitable for high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum, reduced filter requirements, and are suitable for renewable and distributed generation system. Using multilevel technique, the amplitude of the output voltage is increased, and the overall harmonic profile is improved. In case of Switched capacitor multilevel inverter, the topology is cascaded by a DC-DC multilevel converter and a full bridge. For its DC-DC converter section consists of the number of n SC cells, it is capable of providing a number of n+1 voltage levels according to different switching states [1]. With the operation of the H-bridge, a total of 2n+3 voltage levels can be produced.

Neutral point clamped (NPC) multilevel converters have also been found to have excellent performance in terms of output voltage waveform quality, higher compatibility for medium voltage applications, lower electromagnetic interference, reduced common mode voltage, lower voltage stress across the semiconductor devices and improved line-current-distortion [2]. Due to aforementioned qualities, NPC inverters have found applications in wide areas including medium voltage drives, renewable energy, traction and marine propulsion. But it's observed that, NPC topology introduces lower order harmonics in an NPC fed IM operated at low switching frequency [2].

Among these MLI topologies, one of the most competitive topology is a Packed U Cell (PUC) MLI, It consists of packed U cells (PUC). Each U cell consists of an arrangement of two power switches and one capacitor. It offers high-energy conversion quality using a small number of capacitors and power devices and consequently, has a very low production cost. But the topology suffers from complex control strategy [11].

The basic two level inverter output has high harmonic distortion content and cannot be used for high power applications and drive systems hence, multilevel inverters can be used to replace the two level inverters. For a particular switching frequency, compared with a two level inverter, the harmonic content is less in case of MLI. The multilevel inverters have been developed and utilized for higher voltage levels. Using multilevel technique, the amplitude of the output voltage is increased, switching stress in the devices is reduced and the overall harmonic profile is improved.

Cascaded MLIs are constructed by linking in series output terminals of several H-bridge inverters. [8] It is hence evident that this configuration supports high power levels with the use of low voltage rating components in inverters. In case of a fault in any one of the inverter cells, it can be easily and quickly replaced because of its modularity property. In order to maintain reliability in inverter output in the event of a fault in any inverter cell, a suitable control strategy can be used to bypass the faulty cell without disturbing the load. With advancements in multilevel inverters, the need for the design of new modulation methods for the same is increasing [8]. As a result, many modulation schemes have been introduced. Based on converter topology and its domain of application, each modulation technique has its own advantages and

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disadvantages. The PWM switching is suitable for Hybrid cascaded MLI.

The cascaded MLI can be operated in both symmetric and asymmetric configuration. In the symmetric configuration, the magnitude of input DC sources is equal, due to which a number of output levels are less in addition to utilizing more number of switches with increased total harmonic distortion (THD). In contrast, asymmetric MLI input DC sources are unequal due to which different voltage levels can be generated. By combining such voltage levels more levels can be generated with a lesser number of switches with a consequent reduction in THD.

Induction motors are dominantly used in industries due to their merit on cost and reliability [12]. The inverters feeding induction motor plays a major role in improving the performance of the drive system. When compared with basic three phase VSI fed induction motor drive, the multilevel inverter fed drive system exhibits improved performance, as there is reduction in total harmonic distortion in machine currents, transients in electromagnetic torque and transient time period.

II. CASCADED H BRIDGE MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

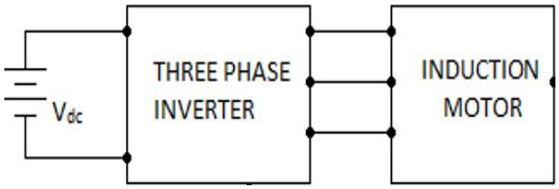

Fig 1:- Block Diagram of Induction Motor Drive

Figure above depicts the block diagram of Cascaded H Bridge multilevel inverter fed induction motor drive. The input DC supply is given to three phase inverter and is used to drive an induction motor.

The circuit of a single phase Cascaded H Bridge Multilevel Inverter (MLI) is shown in figure 2. The first stage is a level generator, which generates the unipolar multilevel voltage waveforms by utilizing the half bridge module. In reality, the DC-power supplies can be battery sources, or rectifier output terminals. [8]

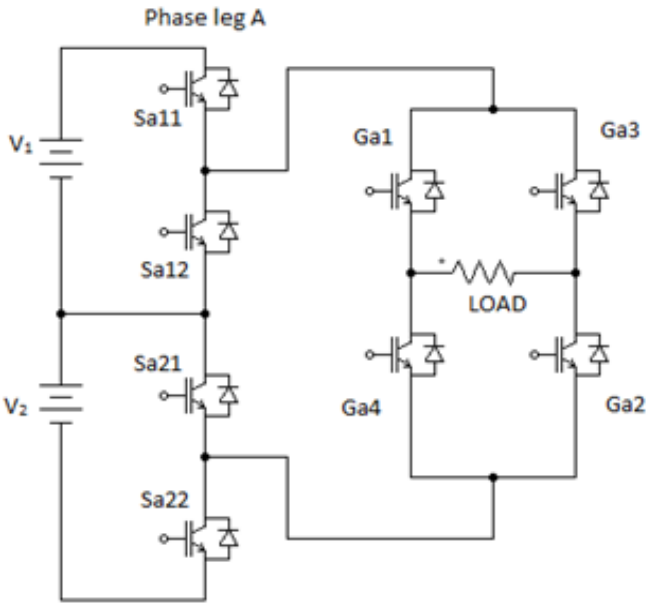

Fig 2:- Cascaded H Bridge Multilevel Inverter

In the circuit switches S_{a11}, S_{a12}, S_{a21}, S_{a22}, are the switches for level generation .G_{a1}, G_{a2}, G_{a3} and G_{a4} are switches in the H Bridge section.

Level	S_{a11}	S_{a12}	S_{a21}	S_{a22}	G_{a1} ,G_{a2}	G_{a3} , G_{a4}
0 V	0	1	1	0	1	0
V_{dc}	1	0	1	0	1	0
2 V_{dc}	1	0	0	1	1	0

Table 1:- Switching States

Table 1 shows the various switching states of Cascaded H Bridge MLI topology. Switches S_{a12} , S_{a21} , G_{a1} ,G_{a2} are turned on to obtain 0 V. V_{dc} is obtained when switches turned S_{a11} , S_{a21} , G_{a1} ,G_{a2} are turned ON. And for 2 V_{dc} the switches S_{a11} , S_{a22} , G_{a1} ,G_{a2} are turned ON .Similarly in the negative halfcycle , V_{dc} is obtained when switches S_{a11} ,S_{a21} ,G_{a3} ,G_{a4} are ON.And for 2 V_{dc} the switches S_{a11} , S_{a22} , G_{a3} ,G_{a4} are turned ON.

III. SIMULATION OF CASCADED H BRIDGE MLI

The Cascaded H Bridge Multilevel inverter is simulated in MATLAB/SIMULINK R2017a with an input of 120V and output is obtained as 230 V .The switching frequency is taken as 1KHz . Figure 2. Shows the 5 level voltage and current waveforms for the inverter topology with a resistive load of 1Ω.

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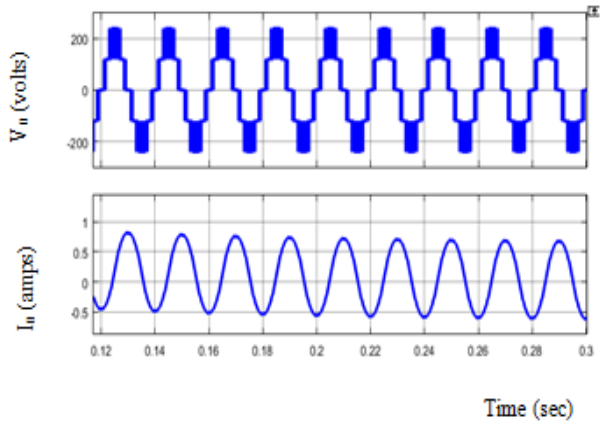

Fig 3:- Output Voltage and Current Waveforms with RL(R = 5Ω,L=1H) Load

The load is now changed into inductive load and figure 3 shows the output voltage and current waveforms with RL load at R = 5Ω and L=1H.The current is observed to be a continuous waveform at inductive load.

Now the inverter is used to drive the induction motor. The rotor angle, electromagnetic torque and speed is observed.When compared with basic three phase voltage source inverter ,the THD in machine currents and transients are reduced.The speed settles to 1500 rpm after transient of 0.2sec.

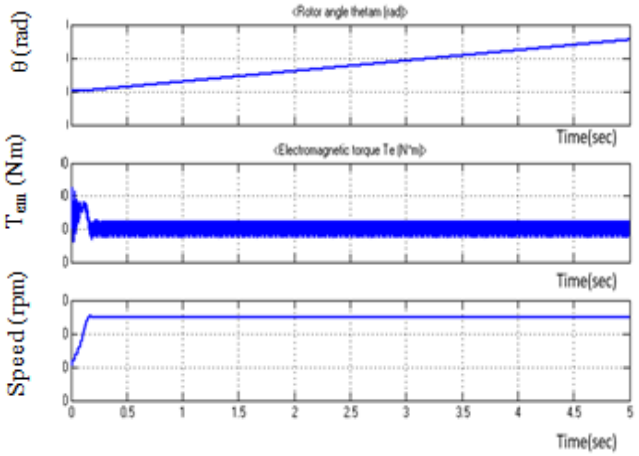

Fig 4:- Output Waveforms of Induction Motor Drive

IV. PERFORMANCE ANALYSIS

For analysis of the converter, it is assumed that all the components are ideal and the system is under steady state.

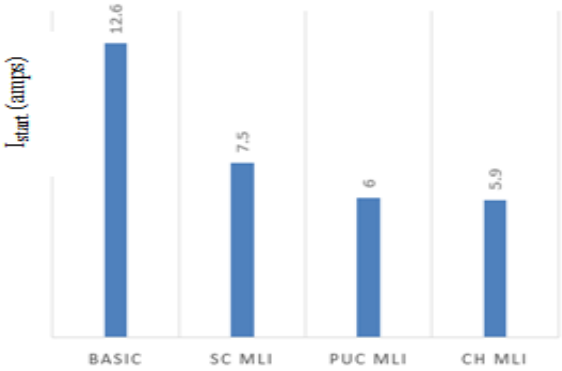

Fig 5:- Starting Current Vs MLI Topologies

Various Multilevel inverter topologies including a Switched Capacitor MLI , Packed U cell MLI and Cascaded H Bridge MLI are compared with basic three phase inverter and from Fig 4, It is observed that, the starting current is reduced in a cascaded H Bridge MLI when compared with basic inverter topologies.About 46 % of reduction in starting current is obtained for MLI topologies.

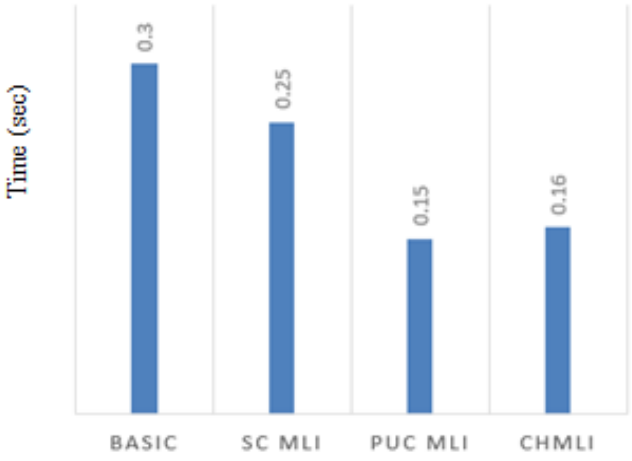

Fig 6:- Voltage Stress Versus Duty Cycle

Figure 5 shows the comparison of transient period of various MLI topologies. It is observed that the transient period is comparitively lower in cascaded H Bridge MLI.

Components	Basic	SCMLI	PU Cell	C H bridge
Number of Input Voltage sources	1 (400 V each)	3 (200 V each)	3 (400 V each)	2 (200 V each)
THD	31 %	25 %	28 %	31 %
Number of switches	6	18	18	24

Table 2:- Comparison of Various MLI Topologies

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Table 2 gives the comparison interms of the number of input voltage sources , THD and starting currents.The number of input dc sources are more in MLI topologies when compared to basic three phase VSI.

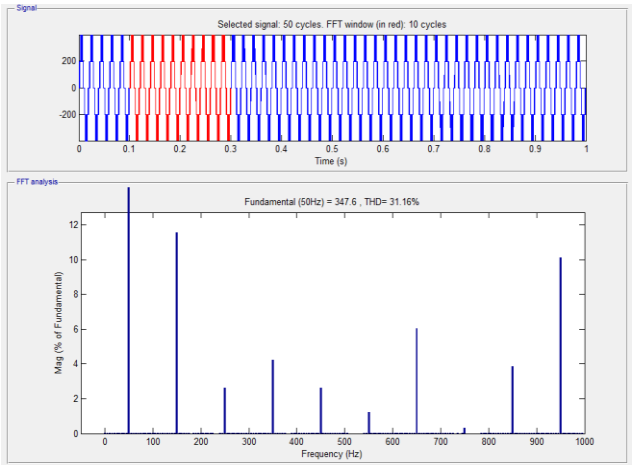

Fig 7:- FFT Analysis of Cascaded H Bridge MLI

In terms of THD and starting currents ,the MLI topologies are superior.Figure 6 depicts the FFT analysis of cascaded multilevel inverter.From the FFT analysis , its observed that ,the total harmonic distortion is about 31 % for cascaded H Bridge MLI topology also ,when compared to other topologies,the variation in output voltage with variation in load conditions are comparitively minimum for cascaded H Bridge MLI topology.

	Basic	SCMLI	PU Cell	C H bridge
Transient period	0.3 s	0.3 s	0.15 s	0.15 s
Transient in T_{em} (Nm)	150	150	300	200
Stator Current	20	120	150	150

Table 3:- Comparison of Various MLI Fed IM Drive

Table 3 depicts the comparison of various MLI fed IM drives. The starting current is reduced to about 46 % for Multilevel inverter topologies when compared to that of a basic three phase inverter.

V. LOSSES

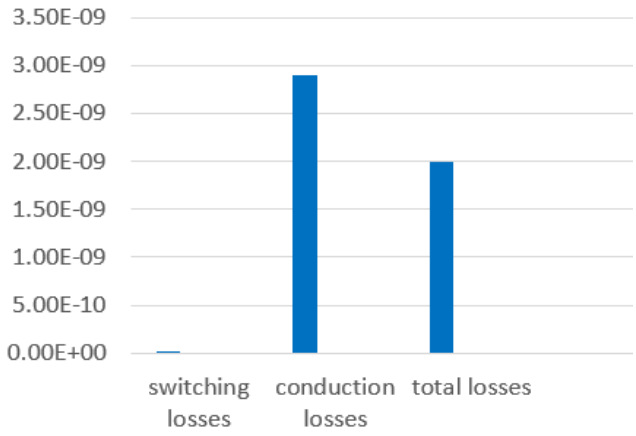

Fig 8:- Losses of the MLI

The total losses will be equal to the sum of switching and conduction losses of the semiconductor devices and is obtained as 2 * 10 $^{-9}$ W. Figure shows the losses of the cascaded H Bridge MLI topology.

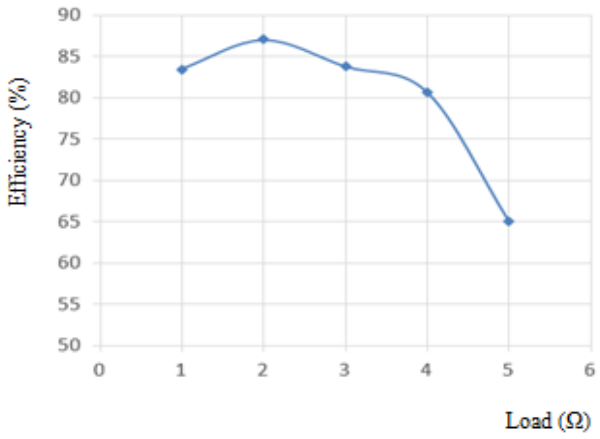

Fig 9:- Efficiency vs R Load Curve

It is observed that ,the efficiency is maximum at resistive load of 5 Ω . Figure 10 shows the Efficiency vs R load curve. The efficiency linearly increases initially and at a load of 100 k, it reduces to about 21 % .

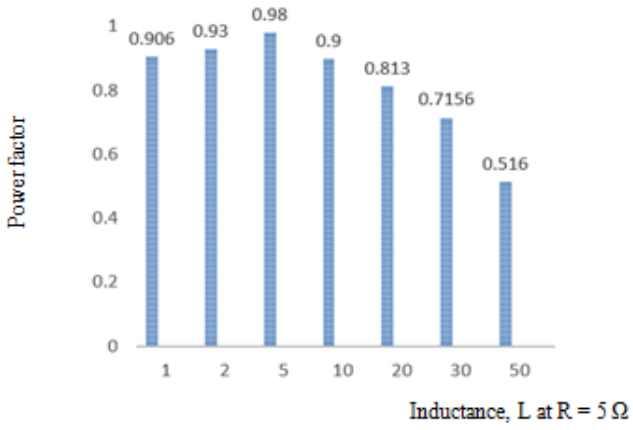

Fig 10:- Power Factor vs. RL Load

Figure shows the Powe factor Vs. Load curve of the inverter topology.As the maximum efficiency is obtained at R = 5Ω ,hence R is fixed at 5 Ω and for different values of L ,power factor is calculated. Its observed that , at 5mH,the power factor is about 0.98.

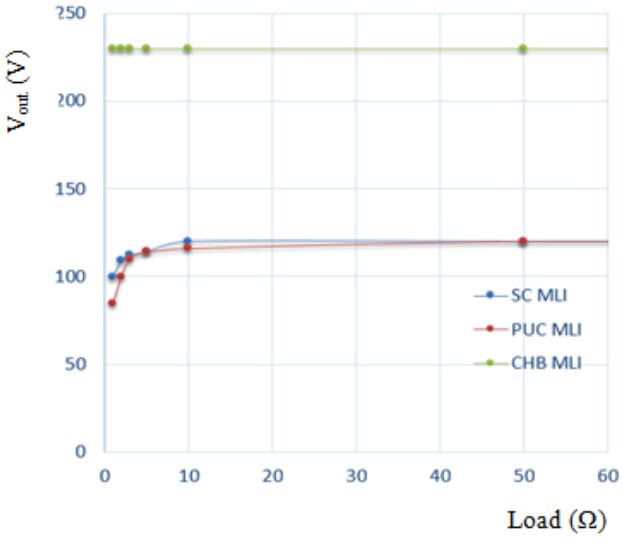

Fig 11:- Output Voltage vs Load Curve

Figure 11 depicts the variation in output voltage along with load variations for different inverter topologies ,when simulated at an input voltage of 120 V. It is observed that,for various MLI topologies including Switched capacitor MLI and Packed u cell MLI,the output voltage varies along with load variations.Whereas for a cascaded H Bridge MLI topology,the output voltage is almost constant for variations in the load.

VI. STABILITY ANALYSIS

For analyzing the stability of the inverter topology, it's assumed that the inverter is an "Ideal inverter". Means the internal inductance, resistance, and capacitance of the switches can be neglected. [9] Then we can just analyze the output filter. Where R_d forms the damping resistance. R_d along with LC filter is used to damp the resonance.

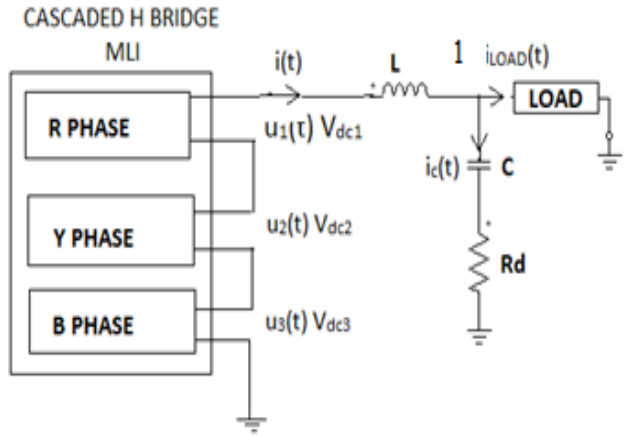

Fig 12:- Circuit Arrangement for Stability Analysis

On applying KVL;

$$L\frac{di}{dt} + V(t) = U_1(t)\,V_{dc1} + U_2(t)\,V_{dc2} + U_3(t)\,V_{dc3} \quad (1)$$

Let

$$, U_1(t)\,V_{dc1} + U_2(t)\,V_{dc2} + U_3(t) = \sum_{k=1}^{3} U_k(t) V_{dck} = g(t)$$

that is ; $L\frac{di}{dt} + V(t) = g(t)$ (2)

On applying KCL at node 1 ;

$$i_c(t) = i(t) - i_{load}(t) \quad (3)$$

Where , Current through capacitor ,

$$i_c(t) = C\frac{dV(t)}{dt} - C\frac{dR_d i_c(t)}{dt}$$

$$and\ current\ through\ Load\ , \qquad i_{load}(t) = \frac{V(t)}{R}$$

Then eq (3) becomes ;

$$i_c(t) = C\frac{dV(t)}{dt} - C\frac{dR_d i_c(t)}{dt} = i(t) - i_{load}(t) \quad (3)$$

i(t) can be calculated from eq(2) as ;

$$i(t) = \int \frac{g(t)}{L}\,dt - \int \frac{V(t)}{L}\,dt$$

Substituting in eq (3) ,we get ;

$$\int \frac{g(t)}{L}\,dt - \int \frac{V(t)}{L}\,dt - \frac{V(t)}{R} = C\frac{dV(t)}{dt} - C\frac{d\,R_d}{dt}\left[\int \frac{g(t)}{L}dt - \int \frac{V(t)}{L}dt - \frac{V(t)}{R}\right] \quad (4)$$

Upon linearizing equation (4) using perturbation technique and adding small signal variation component ; we get ;

$$\frac{1}{L}\sum_{k=1}^{n}[U_k + U_{k1}(t)]\,V_{dc}k + C\frac{R_d}{L}\frac{d}{dt}\left[\sum_{k=1}^{n}[U_k + U_{k1}(t)]V_{dc}\,k\right] = C\frac{d^2}{dt^2}[V + V_1(t)] + \frac{1}{R}\frac{d}{dt}[V + V_1(t)] + C\frac{R_d}{R}\frac{d^2}{dt^2}[V + V_1(t)] + C\frac{R_d}{L}\frac{d}{dt}[V + V_1(t)] + \frac{1}{L}[V + V_1(t)] \quad (5)$$

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From eq (5) separating constant part and small signal part , and when assuming the small signal variations are assumed to be within tiny range , we get ,

$$\frac{1}{L}\,U(t)\sum_{k=1}^{n}\varepsilon_k\,V_{dc}k+\;C\;\frac{R_d}{L}\;\frac{d}{dt}\;[U_{k\,1}](t)\sum_{k=1}^{n}\varepsilon_k\,V_{dc}k = C\;\frac{d^2V_1(t)}{dt^2}+C\;\frac{R_d}{R}\frac{d^2V_1(t)}{dt^2}+\frac{1}{R}\frac{d\,V_1(t)}{dt} + C\;\frac{R_d}{L}\;\frac{d}{dt}\;V_1(t) + \frac{1}{L}\;V_1(t)$$

On rearranging ,

$$G(s)=\frac{V_1(s)}{U_1(s)}=\frac{(1+CR_d\,S)\sum_{k=1}^{n}\varepsilon_k\,V_{dc}k}{S^2\left(LC+\frac{LC\,R_d}{R}\right)+S\left(CR_d+\frac{L}{R}\right)+1} \qquad (6)$$

Equation 6 gives the small signal model.Now,the transfer function is given by ;

$$\frac{V_1(s)}{U_1(s)}=\frac{K\;(1+CR_d\;S)}{S^2\left(LC+\frac{LC\;R_d}{R}\right)+S\left(CR_d+\frac{L}{R}\right)+1}$$

For the frequency response analysis , replace s = jϖ and K = 1 and typical values for C = 5μF ,R = 10kΩ and R_d = 25 Ω .Inductance value is choosen to be 20 mH.[9]

$$G(s)=\frac{1250\,s+10^7}{S^2+1270\,S+10^7}$$

By Routh Hurwitz Criterion of stability analysis,it can be observed that ,in the first column of routh array , all the elements are positive and there is no sign change . Hence the roots are lying on the left half of S-plane and system is stable

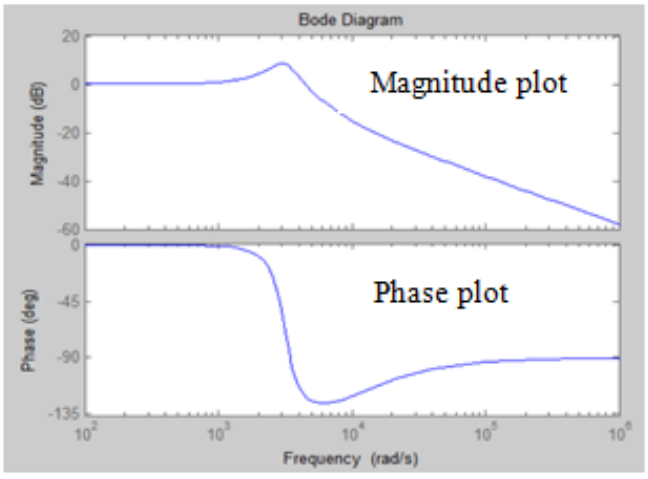

Fig 13:- Bode Plot

From the transfer function , damping ratio ς = 0.2 , hence 0 < ς < 1 and the system is underdamped.

From the transfer function, the bode plot of the topology is obtained as shown in figure 8.For the typical values of filter parameters ,the magnitude plot crosses zero point , Since the magnitude plot crosses zero point ,the corresponding gain cross over frequency is 10^4 rad/sec. But the phase plot does not cross 180 degree due to attenuated phase [10] .

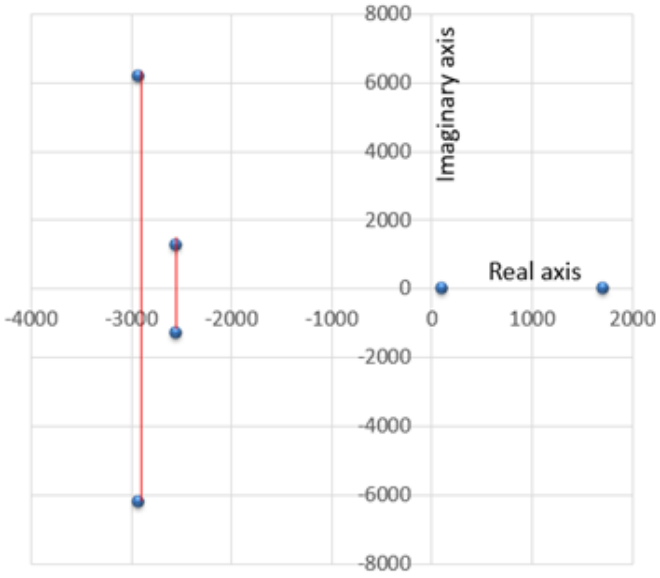

Fig 14:- Trajectory of Eigen Values

Figure 14 depicts the trajectory of eigen values at different filter inductances. It can be concluded that, from 4mH to 7mH the system is stable. As the inductance is increased beyond 7mH, the eigen values shift toward the right half of s plane, making the system oscillatory and unstable.

VII. HARDWARE IMPLEMENTATION

The gate pulses are generated using TMS320f28335 DSP Processor. It's based on Harvard Architecture with a high performance 32 bit CPU, with an on chip memory of 256K × 16 Flash, 34K × 16 SARAM. Figure 9 shows the hardware setup.

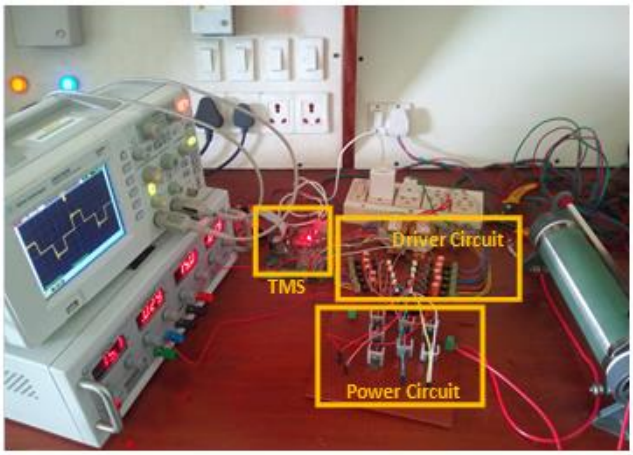

Fig 15:- Hardware Setup

Figure 10 shows the Output Voltage of three level Cascaded H Bridge Multilevel inverter with R (=20 Ω) Load and at an input voltage of V_{in}=30 V.

Fig 16:- Output Voltage

VIII. CONCLUSION

Three phase multilevel inverter fed induction motor drive is designed, employing Cascaded H-Bridge multilevel inverter. A detailed analysis on the multilevel inverter fed induction motor is carried out. When compared with other MLI topologies, the Cascaded H-Bridge multilevel inverter topology have simple control strategy and also, the output voltage will be almost constant for variations in the load. The maximum efficiency of the inverter topology is about 87 %. It is observed that the starting current is reduced to about 46 % when compared to other multilevel topologies. And the THD is reduced to 31 %. From stability analysis, it is observed that all roots of characteristic equation are lying on the left half of S-plane and hence the system is stable. The performance study of induction motor drive is carried out with MATLAB/SIMULINK R2014.The transient period is reduced from 0.5sec to 0.4sec. Peak transient in torque is reduced from 2 Nm to 1.2 Nm and that in current is reduced from 2 A to 0.45 A. There is a considerable reduction in the transient period and THD in the machine currents, are reduced to about 16.8 % while employing multilevel inverters in drive applications. A hardware prototype of the Cascaded H Bridge MLI is developed. At an input voltage of 30 V dc , an output of 30V ac is obtained.

REFERENCES

[1]. Yuanmao Ye, Hirotaka Koizumi,“A Step-Up Switched Capacitor Multilevel Inverter with Self Voltage Balancing”, IEEE Transactions on Industrial Electronics, vol. 59, no.2, February 2013.

[2]. Akira Nabae, Isao Takashi, ”A New Neutral-Point-Clamped PWM Inverter” IEEE transaction on industrial applications,Vol. IA-17, No. 5. September/October 1981.

[3]. Jos Rodrguez, Jih-Sheng Lai and Fang Zheng Peng,” Multilevel Inverters: A Survey of Topologies,Controls, and Applications” IEEE transaction on industrial electronics Vol. 49, No. 4, August 2002.

[4]. Fang Z Peng,” A generalized multilevel inverter topology with self voltage balancing” IEEE transaction on industrial electronics Vol. 49, No. 4, August 2000.

[5]. P.Thongprasri, “ A 5-level three-phase Cascaded hybrid Multilevel Inverter” International journal of computer and electrical engineering, vol. 3, no. 6, Dec 2011.

[6]. S .Raghuram Rajan ,” Multi-Input Switched-Capacitor Multilevel Inverter for High-Frequency AC Power Distribution” IEEE transaction on industrial applications,September 2017.

[7]. Youssef Ounejjar ,” Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation” Ieee Transactions On Industrial Electronics, Vol. 58, No. 4, April2011

[8]. Hasan,” A Three-Phase Symmetrical DC-Link Multilevel Inverter with Reduced Number of DC Sources”, IEEE Transactions on Power Electronics, vol. 59, no.2, February 2017.

[9]. Davi Curi “Simplified Small-Signal Model for Output Voltage Control of Asymmetric Cascaded HBridge Multilevel Inverter”IEEE Transactions 2017

[10]. Fang” An Improved Virtual Inertia Control for ThreePhase Voltage Source Converters Connected to a Weak Grid” IEEE Transactions on Power Electronics,2018

[11]. Youssef Ounejjar “Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation” Ieee Transactions On Industrial Electronics, Vol. 58, No. 4, April2011

[12]. K. Sivakumar “Multilevel Inverter Scheme for Performance Improvement of Pole Phase Modulated Multiphase Induction Motor Drive” ieee transactions on industrial electronics,2015